



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Parulkar et al.  
SERIAL NO.: 10/611,467  
FILING DATE: June 30, 2003  
TITLE: ON-CHIP TESTING OF EMBEDDED MEMORIES USING  
ADDRESS SPACE IDENTIFIER BUS IN SPARC ARCHITECTURES  
ART UNIT: 2184  
EXAMINER: [not yet assigned]

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**CERTIFICATE OF MAILING**

I hereby certify that this paper is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Office of Initial Patent Examination's Customer Service Center, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on the date printed below:

Date: 10/21/03 Name: Diane Morse  
Diane Morse

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**REQUEST TO CORRECT FILING RECEIPT**

It is respectfully submitted that the Filing Receipt for the above-identified patent application has several errors.

The address for inventor Chitresh C. Narasimhaiah should read - - San Jose, CA - - and not "San Jode, CA".

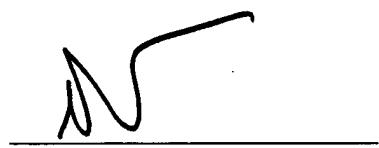
The title should read - - On-Chip Testing of Embedded Memories Using Address Space Identifier Bus in SPARC Architectures- -, and not "On-Chip Testing of Embedded Memories Memories Using Address Space Identifier Bus in SPARC Architectures".

Attached is a copy of the Combined Declaration and Power of Attorney with the title and inventor information, which was filed with the application. Please make the appropriate corrections.

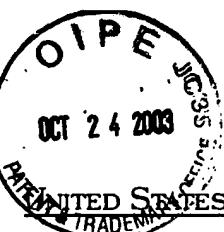
The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to Deposit Account No. 50-1698. A duplicate copy of this page is enclosed.

Respectfully submitted,  
THELEN REID & PRIEST LLP

Dated: 10/20, 2003

  
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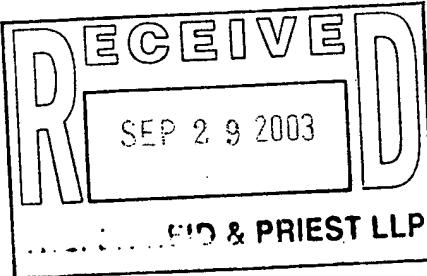
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APPL NO.	FILING OR 371 (c) DATE	ART UNIT	FIL FEE REC'D	ATTY.DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/611,467	06/30/2003	2184	834	SUN-P8374	3	19	4

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 San Jose, CA 95164



CONFIRMATION NO. 1597

## FILING RECEIPT



\*OC000000010909656\*

Date Mailed: 09/23/2003

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

## Applicant(s)

Ishwardutt Parulkar, San Francisco, CA;  
 Chitresh C. Narasimhaiah, San Jose, CA;  
 Jose.

## Assignment For Published Patent Application

Sun Microsystems, Inc. a Delaware Corporation;

## Domestic Priority data as claimed by applicant

## Foreign Applications

If Required, Foreign Filing License Granted: 09/23/2003

Projected Publication Date: 12/30/2004

Non-Publication Request: No

Early Publication Request: No

Reviewed By: MP Date: 10/3/03

No Action Required:

Action Required: *✓ Title & Inventor Residence misspelled*

Mail log \_\_\_\_\_ Date \_\_\_\_\_

CPI \_\_\_\_\_ DOCKETED \_\_\_\_\_  
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Excel \_\_\_\_\_ Date \_\_\_\_\_

## Title

On-chip testing of embedded memories using Address Space Identifier bus in SPARC architectures

Preliminary Class

714

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Title 35, United States Code, Section 184  
Title 37, Code of Federal Regulations, 5.11 & 5.15**

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